a lower electrode containing Pt provided over said insulation film;

a PZT ferroelectric film provided on said lower electrode, said PZT ferroelectric film having a columnar microstructure extending from an interface between said lower electrode and said PZT ferroelectric film in a direction substantially perpendicular to a principal surface of said lower electrode, said PZT ferroelectric film consisting of crystal grains having a substantially uniform grain diameter of less than about 200 nm; and

an upper electrode provided on said PZT ferroelectric film.

REMARKS

This response addresses the Office Action dated June 19, 2002, in which claims 1, 2, 4-19 and 21-28 remain pending, except for claim 13 which is now cancelled.

Claims 1, 2, 4-19 and 21-28 stand rejected under 35 USC 103(a) as being unpatentable over the combination of Cuchiaro et. al (US Patent No. 6,165,802), Chu et. al (US Patent No. 6,287,637), and Izuha et. al (US Patent No. 6,060,735).

The rejection of claims 1, 2, 4-19 and 21-28 under 35 USC 103(a) is respectfully traversed.

As previously noted, Cuchiaro et. al merely describes a background art method of fabricating a ferroelectric integrated circuit and is entirely silent about the feature of the annealing process of a PZT film as set forth in the claims of the present invention, in which the PZT film is first crystallized in an ambient of a non-oxidizing gas and an oxidizing gas, and with a specific range for the proportion of the oxidizing gas. Further, Cuchiaro is silent about the second annealing process conducted in an ambient of an oxidizing gas.

It is noted that the newly cited reference to Chu et. al describes a two-step annealing process of a PZT film in which an ambient of low oxygen partial pressure is used for the first annealing step. Further, Chu et. al teaches the use of an ambient of argon and oxygen for the first annealing step.

On the other hand, claims 1 and 21 of the instant invention describes a

specific range of oxygen concentration of 1 to 20% for achieving the optimized electric performance of the ferroelectric capacitor. With regard to this feature, we note that the Examiner argues that Chu et. al inherently teaches that the oxygen gas must be with a fraction of 1 to 20% in volume.

Chu et. al merely teaches the reduction of the oxygen partial pressure in the first annealing step as noted above. While there is a description in Chu et. al that "[t]he oxygen partial pressure in Ramtron's RTA ... chamber is in the range of 10^{-4} to 100 Torr" (column 7, lines 26 to 28), this does not mean at all that the preferable range of oxygen concentration in the ambient to be used for the first annealing step is in the range as claimed in claims 1 and 21.

Chu et. al is not specific about the oxygen partial pressure used in the experiments of FIGS. 2a-2d thereof. Further, Chu et. al does not mention that the oxygen partial pressure is controlled in their experiments of FIGS. 2a-3d.

Thus, it is deemed that the preferable range of oxygen concentration claimed in claim 1 or claim 21 is not described or even suggested in Chu et. al and that the subject matter of claim 1 or claim 21 cannot be derived from Chu et. al, even when combined with Cuchiaro et. al and Izuha et. al. In the present invention, the preferable range of the oxidizing gas is clearly supported by FIGS. 13-18 and related description.

Thus claims 1 and 21 are deemed to be allowable over the combination of cited prior art. Claims 12 and 14 are also deemed to be allowable for the same reasons given above. Further, claims 2, 4-11 and claims 23-28 dependent from claim 1 or claim 21 are also deemed to be allowable.

Claim 15 recites that the columnar grains have a generally uniform grain diameter, which is not described or suggested in Izuha. It is important to note that FIG. 4A of Izuha is a schematic diagram and does not represent the grain diameter to scale. FIG. 4B of Izuha is a TEM photograph. As best as can be determined from the print of FIG. 4B, the film of Izuha does not show the claimed feature that the columnar grains have a generally uniform grain diameter.

In contradistinction to Izuha, the photographs of FIGS. 7A and 7B in the

present application clearly show the microstructure that supports the subject matter of claim 15. Particularly, the cross-sectional fracture surface of FIG. 7B shows that the crystal grains have a substantially identical grain diameter as claimed.

Claim 15 is thus deemed to be allowable as distinguishing over the cited prior art combination. Claims 16-19 are also deemed to be allowable as depending from allowable base claim 15.

In view of all of the above, claims 1, 2, 4-12, 14-19 and 21-28 are believed to be allowable and the case in condition for allowance which action is respectfully requested. Should the Examiner be of the opinion that a telephone conference would expedite the prosecution of this case, the Examiner is requested to contact Applicants' attorney at the telephone number listed below.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version with Markings to Show Changes Made."

A Request for Two-Month Extension of Time is included with this Amendment. No further fees are believed due, however, any fee deficiency associated with this submittal may be charged to Deposit Account No. 50-1123.

Respectfully submitted,

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Peter Meza

Peter J. Meza, No. 32,920
Hogan & Hartson LLP
One Tabor Center
1200 17th Street, Suite 1500
Denver, Colorado 80202
(719) 448-5906 Tel
(303) 899-7333 Fax

"Version with Markings to Show Changes Made"

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IN THE CLAIMS:

Please amend claims 12, 14, and 15 to read as follows:

12. (Amended) A method of fabricating a semiconductor device having a ferroelectric capacitor, comprising the steps of:

forming an active device element on a substrate;

forming an insulation film over said substrate to cover said active device element;

forming a lower electrode layer of said ferroelectric capacitor over said insulation film;

forming a ferroelectric film on said lower electrode as a capacitor insulation film of said ferroelectric capacitor;

crystallizing said ferroelectric film by applying a thermal annealing process in an $\underline{O_2}$ atmosphere [of an oxidizing gas] under a reduced total pressure [smaller than an atmospheric pressure] <u>in the range between 1 Torr and 40 Torr</u>; and

forming an upper electrode layer on said ferroelectric film.

14. (Amended) A method of fabricating a semiconductor device having a ferroelectric capacitor, comprising the steps of:

forming an active device element on a substrate;

forming an insulation film over said substrate to cover said active device element;

forming a lower electrode layer of said ferroelectric capacitor over said insulation film, said lower electrode layer including a layer part containing Ti atoms;

forming a ferroelectric film on said lower electrode layer as a capacitor

insulation film of said ferroelectric capacitor;

crystallizing said ferroelectric film by applying a thermal annealing process in an atmosphere of an oxidizing gas with a fraction of 1 to 20% in volume; and

forming an upper electrode layer on said ferroelectric film,

wherein said step of crystallizing said ferroelectric film is conducted by supplying O_2 controlled to cause an oxidation in said Ti atoms reached a surface of said lower electrode from said layer part containing Ti atoms.

15. (Thrice Amended) A semiconductor device, comprising:

a substrate;

an active device element formed on said substrate;

an insulation film provided over said substrate to cover said active device element;

a lower electrode containing Pt provided over said insulation film;

a PZT ferroelectric film provided on said lower electrode, said PZT ferroelectric film having a columnar microstructure extending from an interface between said lower electrode and said PZT ferroelectric film in a direction substantially perpendicular to a principal surface of said lower electrode, said PZT ferroelectric film [essentially] consisting of crystal grains having a [generally] substantially uniform grain diameter of less than about 200 nm; and

an upper electrode provided on said PZT ferroelectric film.